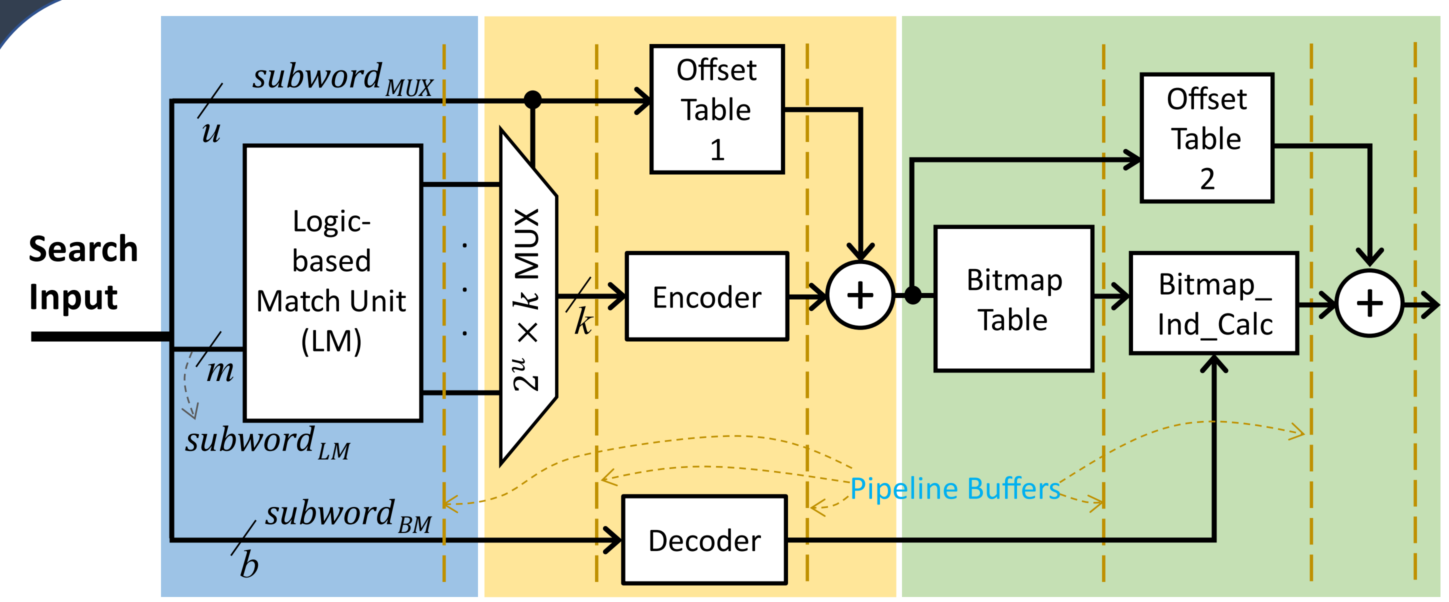
DSCAM: Latency-Guaranteed and High-Capacity Content Addressable Memory on FPGAs

INRS Institut national de la recherche scientifique

ECCoLe Edge Computing, Communication and Learning Lab

- ✓ An innovative approach to implement content-addressable memory on FPGA
- ✓ High-throughput, short and fixed latency
- ✓ Cost-effective: enables implementing large search tables on budget-friendly FPGAs
- ✓ Adjustable trade-off between logic resource and SRAM utilization based on the design priorities

Hardware Architecture

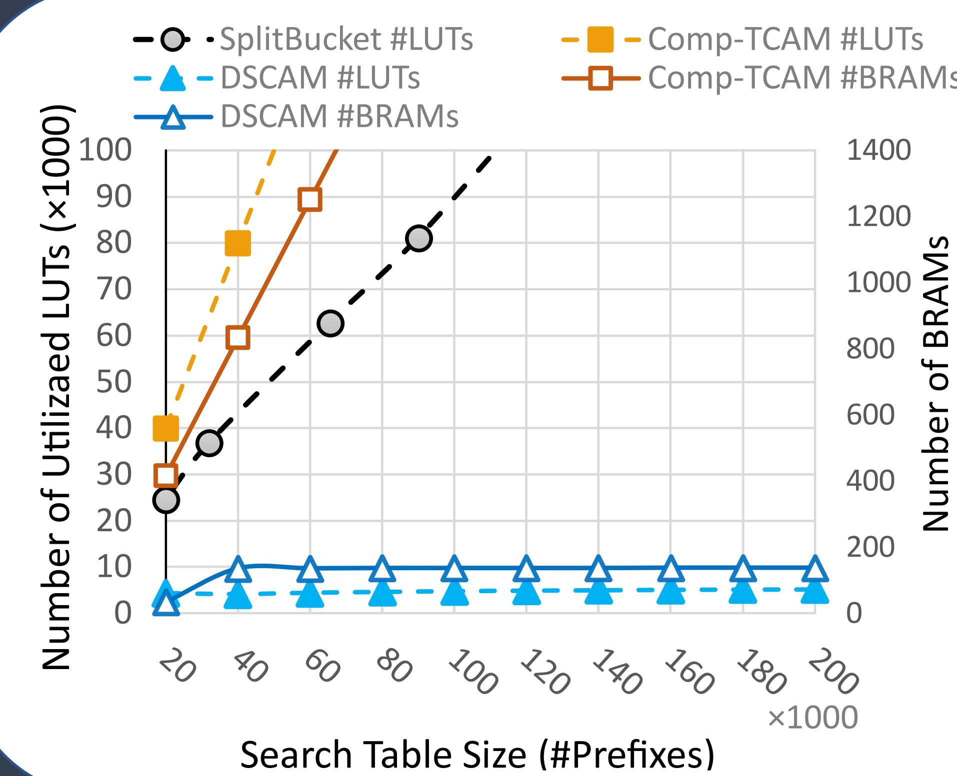


✓ Fully Pipelined

Logic-Based Match Stage (ML) | MUX Stage (MUX) | Bitmapping Stage (BM)

Three stages, each tasked with matching a specific subword of the input.

Results



	DSCAM	
Device	Xilinx Xcku5p Kintex US+	
Table Size	512	524,287
Bitwidth	32	32
LUTs	1.4 K	45.3 K
BRAM (36K)	0	308.5
Max. Freq. (MHz)	675	232
Latency (ns)	8.9	25.9

- ✓ IPv4 forwarding table with >520 K IP prefixes
- ✓ Throughput of > 230 M searches per second

Example

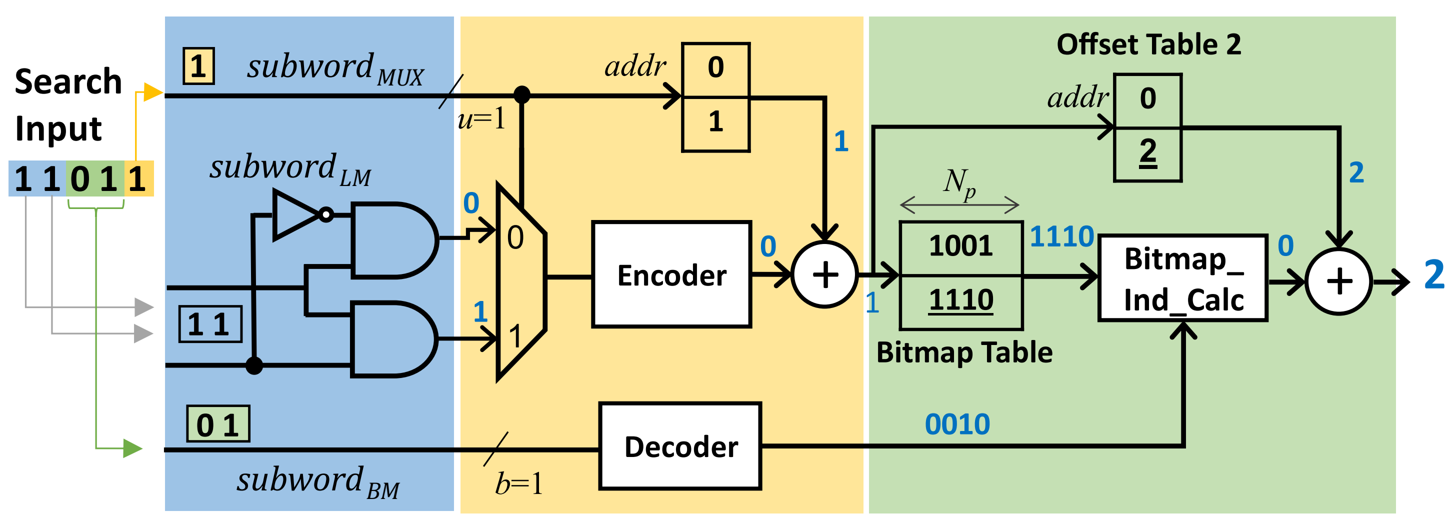
Search Table

0	0	1	0	0	0
1	0	1	1	1	0
2	1	1	0	1	1
3	1	1	1	0	1
4	1	1	1	1	1
	bit_4	bit_3	bit_2	bit_1	bit_0

Subword Partitioning Scheme

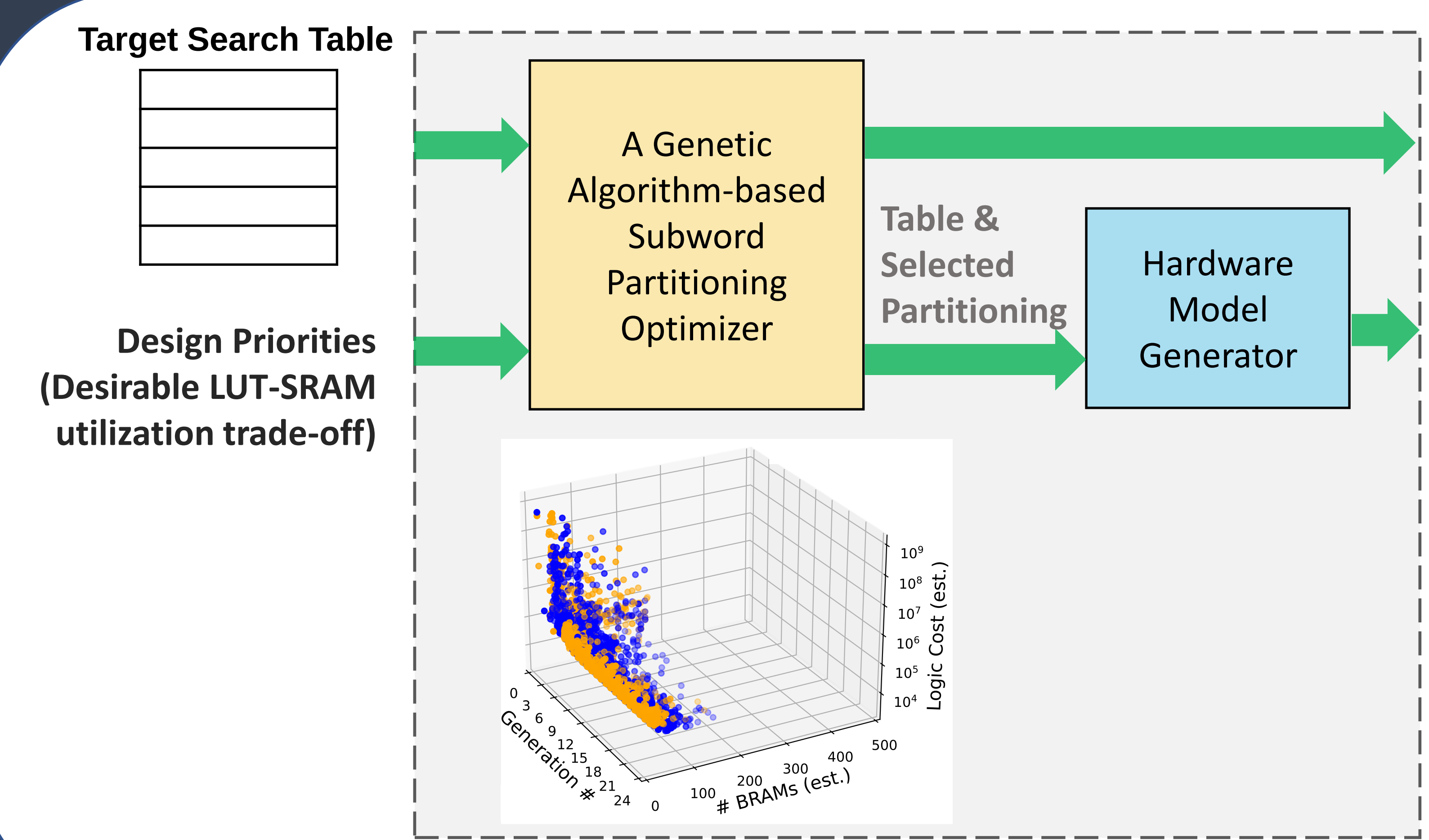
- $subword_{LM}$: bit_4, bit_3 (m=2)
- $subword_{MUX}$: bit_0 (u=1)
- $subword_{BM}$: bit_2 , bit_1 (b=2)

Subword partitioning highly impacts the efficiency of DSCAM hardware.



Logic-Based Match Stage (ML) | MUX Stage (MUX) | Bitmapping Stage (BM)

DSCAM Design Flow



CAD Automated DSCAM Core Generator